HARDWARE LAB 3

# Designing 3-Bit Synchronous Counter Using Flip-Flops

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State Table for the 3-bit synchronous counter:

**Present States Next States Flip-Flop inputs**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| *B*(t) | *C*(t) | *D*(t) | *B*(t+1) | *C*(t+1) | *D*(t+1) | JB | KB | JC | KC | JD | KD |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | X | 1 | X | 1 | X |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | X | 0 | X | X | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | X | X | 1 | 1 | X |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | X | X | 0 | X | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | X | 1 | 1 | X | 1 | X |
| 1 | 0 | 1 | 1 | 0 | 0 | X | 0 | 0 | X | X | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | X | 0 | X | 1 | 1 | X |
| 1 | 1 | 1 | 1 | 1 | 0 | X | 0 | X | 0 | X | 1 |

K-MAPS and Equations:

C

|  |  |  |  |
| --- | --- | --- | --- |
| * 1   B | * 0 | * 0 | * 0 |
| * X | * X | * X | * X |

D

J**B** = C’D’

C

|  |  |  |  |
| --- | --- | --- | --- |
| * X   B | * X | * X | * X |
| * 1 | * 0 | * 0 | * 0 |

D

K**B** = C’D’

C

|  |  |  |  |
| --- | --- | --- | --- |
| * 1   B | * 0 | * X | * X |
| * 1 | * 0 | * X | * X |

D

J**C** =D’

C

|  |  |  |  |
| --- | --- | --- | --- |
| * X   B | * X | * 0 | * 1 |
| * X | * X | * 0 | * 1 |

D

K**C** =D’

C

|  |  |  |  |
| --- | --- | --- | --- |
| * 1   B | * X | * X | * 1 |
| * 1 | * X | * X | * 1 |

D

J**D** =1

C

|  |  |  |  |
| --- | --- | --- | --- |
| * X   B | * 1 | * 1 | * X |
| * X | * 1 | * 1 | * X |

D

K**D** = 1

Logisim Circuit Diagram:

